AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph starting on page 2, line 10 with the following amended paragraph:

--An example of a column amplifier stage is shown in figure 2. The column amplifier stage includes an operational amplifier 206, capacitors 202 and 205 and transistors 210, 212 and 204. The column bit-line COL_j is connected to the source of transistor 210. The column amplifier stage read sequence is described in conjunction with figure 3. Prior to the row access pulse, during the ~~integrationstage~~ integration stage, the Column Access signal CA is a logical low. Once the row is accessed, the row access pulse RA_i is a logical high and the source follower 102 drives the column line 109 to its video signal level. During this time the sampling capacitor 202 and the feedback capacitor 205 are set to a reference voltage V_{REF}. Then the Direct Readout signal DRO switches to a logical low followed by the Column Access signal CA which switches to a logical high. From this point in time, the video level of the column line COL_j is being sampled. Then the Column Reset signal CRS switches to a logical low followed by the Column Access signal CA which switches to a logical low. After Direct Readout signal DRO switches to a logical high the output voltage V_{OUTj} becomes valid until the Column Reset signal CRS switches to a logical high.--

Please replace the paragraph starting on page 11, line 17 with the following amended paragraph:

--The timing of a CMOS imager that uses the circuitry described in figure 8 is shown in detail in figure 9. This diagram is being simplified for description purposes by having the imaging array consist of only four rows, labeled as 0 - 3. In this particular case, four circuits of the type described with reference to figure 8 would be used, one for each of the rows of pixels. The first waveform in the timing diagram shows the number of the row that is being decoded for reset, the first being 0 at time t0. The first NAND gate 805 of the corresponding circuit will output a logical active low once the Reset Enable signal rst_en pulses a logical high as shown at time t1. This will drive

the Reset Signal RST_i for that row logical high and reset all the pixels in row 0. Once the next address is given, shown as row address 1 at time t2, the circuit corresponding to row 1 will reset the pixels in that row once the Reset Enable signal rst_en pulses a logical high a second time as shown at time t3. Meanwhile, row 0 is being integrated as shown by the time ~~labeled T_{INT}~~ labeled t_{INT}. The reset process continues for each row until the end of the array and then begins again at the first row.--

Please replace the paragraph starting on page 12, line 3 with the following amended paragraph:

--Meanwhile, the decoding of the Row Access signals $RAAX_k$ is occuring in the Row Access decoding circuitry and being input to the third AND gate 806 in each of the four circuits. The first AND gate 806 of row 0 will be active once the Row Access Enable signal ra_en pulses a logical high as shown at time t4 as the decoded address is row 0. The pulse ends the integration ~~time, T_{INT}, of the~~ time, t_{INT}, of the pixel for row 0 as shown and the integrated voltage level of the pixel is read out at this time. This process continues for each of the rows until the end of the array at which time the first row, row 0, is again accessed.--